

Amendments to the Claims:

This listing will replace all prior versions, and listing, of claims in the application.

1-13. (Cancelled):

14. (Previously presented): A CMOS image sensor device comprising:
shallow trench isolation regions in a semiconductor substrate, said shallow trench isolation regions separate said device;
a sensor diode in said semiconductor substrate comprising a first terminal and a second terminal;
a plurality of gates for transistors in said CMOS image sensor wherein said gates comprise a conductor layer overlying said semiconductor substrate with an insulating layer therebetween and wherein said transistors include reset transistors;
source/drain regions for said transistors wherein said source regions of said reset transistors are formed in said first terminals of said sensor diodes; and
double diffused sources only in said reset transistor sources to complete an asymmetrical source/drain structure;
wherein said double diffused sources totally overlap said reset transistor sources;
and
said source/drain regions and double diffused sources contact said shallow trench isolation regions.

15. (Previously presented): The device according to claim 14 wherein said double diffused sources are formed by implanting ions into said reset transistor sources wherein said implanting is blocked from other said source/drain regions, and said double diffused sources have a thicker thickness than said source/drain regions.

16. (Original): The device according to claim 14 wherein said sensor diodes first terminals comprise n-type, said source/drain regions comprise n-type, and said double diffused sources comprise n-type.

17. (Original): The device according to claim 14 further comprising:
lightly doped drain extensions are aligned to said gates; and
sidewall spacers on said gates wherein said source/drain regions are aligned to said sidewall spacers.

18. (Cancelled)

19. (Original): The device according to claim 14 wherein said second sensor diode terminal is coupled to ground and wherein said reset transistor drain is coupled to a power supply.

20. (Original): The device according to claim 14 wherein said transistors further include source follower transistors having gates coupled to said reset transistor double diffused sources.